24 Fall ECEN 704: VLSI Circuit Design

Design Post-lab Report

Lab4: Advanced Layout Design Techniques

Name: Yu-Hao Chen

UIN:435009528

Section:601

Professor: Aydin Karsilayan

TA: Troy Buhr

**Description:**

In this lab, we learned to utilize various layout techniques, including guard rings, I/O pads, and ESD protection. By employing these techniques, we can enhance circuit performance by improving matching, reducing interference from external factors, and providing protection against permanent damage

**Design & result**

|  |
| --- |
| Schematic (without I/O pad) |
| 一張含有 螢幕擷取畫面, space 的圖片  自動產生的描述 |
| layout |
| 一張含有 螢幕擷取畫面, Rectangle, 文字, 藝術 的圖片  自動產生的描述 |
| Layout(PMOS) |
| 一張含有 鮮豔, 馬若雷勒藍, 紫色, 螢幕擷取畫面 的圖片  自動產生的描述 |
| Layout(NMOS) |
| 一張含有 螢幕擷取畫面, 鮮豔, 行, 文字 的圖片  自動產生的描述 |
| DRC |
| 一張含有 文字, 螢幕擷取畫面, 軟體, 電腦 的圖片  自動產生的描述 |
| LVS |
| 一張含有 文字, 螢幕擷取畫面, 軟體, 電腦圖示 的圖片  自動產生的描述 |

**I/O pad**

|  |
| --- |
| I/O pad |
| 一張含有 螢幕擷取畫面, 繪圖軟體, 多媒體軟體, 編輯 的圖片  自動產生的描述 |
| I/O pad (n) |
|  |
| I/O pad (p) |
| 一張含有 電子產品, 螢幕擷取畫面, 文字, 電子工程 的圖片  自動產生的描述 |
| DRC |
| 一張含有 文字, 螢幕擷取畫面, 軟體, 陳列 的圖片  自動產生的描述 |

**ESD**

|  |
| --- |
| Adding ESD |
|  |
| layout |
| 一張含有 螢幕擷取畫面, 藝術, 設計 的圖片  自動產生的描述 |
| 一張含有 螢幕擷取畫面, 鮮豔 的圖片  自動產生的描述 |
| DRC |
| 一張含有 文字, 軟體, 電腦圖示, 網頁 的圖片  自動產生的描述 |
| LVS |
| 一張含有 文字, 螢幕擷取畫面, 軟體, 電腦圖示 的圖片  自動產生的描述 |
|  |

**Discussion:**

After consulting with the teaching assistant about the dummy transistors in the floor plan, I finally resolved my question regarding the absence of two additional rows of dummy transistors at the top and bottom of the floorplan. While it is generally advantageous to include these two rows, it is not essential in this instance (or in typical scenarios); their necessity arises primarily in high-speed circuit applications.

In this lab, I believe we learned more about how to manage a complex circuit. By separating the circuit into multiple steps, we can check the Design Rule Check (DRC) and Layout Versus Schematic (LVS) for each step before proceeding to the next. This approach ensures that we do not confront the entire, massive problem all at once, making it easier to debug and fix the circuit.

**Conclusion:**

After completing Lab 4, we learned important layout techniques like ESD protection and guard rings, which enhance circuit performance and reliability. ESD protection helps safeguard components from voltage spikes, preventing damage, while guard rings improve matching and reduce interference from external noise. These techniques make the circuit more robust and less affected by environmental factors, ensuring higher accuracy and long-term durability in various applications.